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10CS74

Seventh Semester B.E. Degree Examination, Dec.2014/Jan.2015
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Define Computer Architecture. Illustrate the seven dimensions of an ISA. **(08 Marks)**

b. Find the die yield for dies that are 1.5 cm on a side and 1.0 cm on a side assuming a defect density of 0.4 per cm^2 and α is 4. **(04 Marks)**

c. Define Amdahl's law. Derive an expression for cpu clock as a function of instruction count. Clocks per instruction and clock cycle time. **(08 Marks)**

2 a. What is pipelining? With neat diagram, explain the classic five stage pipeline for RISC processor. **(08 Marks)**

b. Consider unpipelined processor. Assume that it has a 1 ns clock cycle and that it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations 40%, 20% and 40% respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2 ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from pipeline? **(06 Marks)**

c. Explain different techniques in reducing pipeline branch penalties. **(06 Marks)**

3 a. Explain true data dependence, name dependence and control dependence, with an example. **(05 Marks)**

b. What is Correlating Predictors? Explain with example. **(05 Marks)**

c. With a neat diagram give the basic structure of Tomasulo based MIPS FP unit and explain various fields of reservation station. **(10 Marks)**

4 a. Explain exploiting ILP using dynamic scheduling multiple issue and speculation. **(08 Marks)**

b. Explain Pentium 4 pipeline supporting multiple issue with speculation. **(08 Marks)**

c. Explain in detail, Branch –Target buffers. **(04 Marks)**

PART – B

5 a. Explain the basic schemes for enforcing coherence in a sheared memory multiprocessor system. **(10 Marks)**

b. Explain the Taxonomy of parallel architecture. **(05 Marks)**

c. Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of the original computation can be sequential? **(05 Marks)**

6 a. Explain four memory hierarchy questions, in detail. **(08 Marks)**

b. Explain in brief, the types of basic cache optimization. **(10 Marks)**

c. Define Virtual Memory and describe its features. **(02 Marks)**

7 a. Which are the major categories of advanced optimizations of cache performance? Explain any one in detail. **(10 Marks)**

b. Describe the technique to improve memory performance inside DRAM chip. **(05 Marks)**

c. Explain the process of protecting via virtual machines. **(05 Marks)**

8 a. Explain detecting and enhancing loop level parallelism for VLIW. **(08 Marks)**

b. Explain Intel – IA 64 architecture, with a neat diagram. **(08 Marks)**

c. Write a brief note on predicated instructions. **(04 Marks)**

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